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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,862	07/03/2003	Tomio Iwasaki	500.39912CX1	3833
20457	7590	03/07/2005	EXAMINER	
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-9889			SMOOT, STEPHEN W	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/611,862

Applicant(s)

IWASAKI ET AL.

Examiner

Stephen W. Smoot

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2005 and 11 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-15, 17, 18, 20, 21, 23 and 24 is/are allowed.
- 6) ☒ Claim(s) 16, 19 and 22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/787,528.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to applicant's RCE filed on 11 February 2005.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's amendment filed on 12 January 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Iwasaki et al. (US 2004/0238965 A1).

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Referring to Fig. 8 and paragraphs [0041] to [0046], Iwasaki et al. disclose an interconnect structure with the following features:

- A semiconductor substrate (101) with gate electrodes (108, 109) and source/drain diffusion layers (102, 103, 104, 105);
- An insulating film (113) supporting an interconnect that comprises a conductor film (117) sandwiched between two neighboring films (116a, 116b);
- The conductor film (117) can be copper and the neighboring films (116a, 116b) can be ruthenium, iridium or osmium (see paragraph [0042]); and

- Plugs (115) electrically connecting the conductor film (117) to the diffusion layers (102, 103, 104).

These are all of the limitations set forth in claim 16 of the applicant's invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 19, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronner et al. (US 5,792,703) in view of Psaras et al. (US 4,803,539).

Referring to Fig. 3 and column 3, line 7 to column 4, line 56, Bronner et al. teach a diffusion region (70) formed in a silicon substrate (50) that is adjacent to a gate stack (60) with a metal contact (110) formed through an insulator (85) to electrically connect the gate stack (60) to an overlying metal line (100). The gate stacks have a polysilicon or silicide electrode. The metal can be a copper alloy (see column 4, lines 46-48). These are limitations set forth in claims 19, 22 of the applicant's invention.

However, Bronner et al. do not teach or suggest a gate electrode with ruthenium, iridium, osmium or platinum as a main constituent (a limitation of claim 19), nor do they teach or suggest a multilayered gate electrode with a first conductive film that includes

silicon and with a second conductive film, nearer to the plug, that includes rhodium, ruthenium, iridium, osmium or platinum as a main constituent (limitations of claim 22).

Psaras et al. teach a gate electrode comprising a lower layer of polysilicon (26) and an upper layer (31) of Rh_2Si (i.e. an upper layer with rhodium as a main constituent) (see Fig. 5 and column 12, lines 9-47). Alternatively, the upper layer (31) can be Pt_2Si (see column 10, line 65 to column 11, line 10).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Bronner et al. and Psaras et al. in order to use a polysilicon/ Pt_2Si gate electrode as taught by Psaras et al. Psaras et al. recognize that silicides like Pt_2Si can be used in gate electrodes for making ohmic contacts (see column 1, lines 20-22 and column 10, line 65 to column 11, line 10).

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bronner et al. (US 5,792,703) in view of Hieda et al. (US 6,278,164 B1).

Referring to Fig. 3 and column 3, line 7 to column 4, line 56, Bronner et al. teach a diffusion region (70) formed in a silicon substrate (50) that is adjacent to a gate stack (60) with a metal contact (110) formed through an insulator (85) to electrically connect the gate stack (60) to an overlying metal line (100). The gate stacks have a polysilicon or silicide electrode. The metal can be a copper alloy (see column 4, lines 46-48).

These are limitations set forth in claims 19, 22 of the applicant's invention.

However, Bronner et al. do not teach or suggest a gate electrode with ruthenium, iridium, osmium or platinum as a main constituent (a limitation of claim 19).

Hieda et al. teach a gate electrode that can be ruthenium, iridium, osmium or platinum (see column 10, lines 35-38).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Bronner et al. by using ruthenium, iridium, osmium, or platinum as the gate electrode material, as taught by Hieda et al. Hieda et al. recognize that ruthenium, iridium, osmium or platinum can function as metallic gate electrodes (see column 10, lines 35-38), which are alternative materials to the polysilicon or silicide gate electrodes taught by Bronner et al.

Allowable Subject Matter

7. Claims 13-15, 17-18, 20-21, 23-24 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

- Claim 13 is allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a plug that comprises a main conductive film that includes copper as a main constituent element and an adjacent conductive film formed outside the main conductive film, wherein the adjacent conductive film includes ruthenium, iridium, or osmium as a main constituent;

- Claims 14-15 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a plug that comprises a main conductive film that includes copper as a main constituent element and an adjacent conductive film formed outside the main conductive film, wherein the adjacent conductive film includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent;
- Claims 17-18 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a connection layer that comprises a main conductive film that includes copper as a main constituent element and an adjacent conductive film formed outside the main conductive film, wherein the adjacent conductive film includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent;
- Claims 20-21 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a gate electrode that includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent; and
- Claims 23-24 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a gate electrode that includes a first conductive film that includes silicon and a second conductive

film that includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent.

Response to Arguments

9. Applicant's arguments, see pages 9-11, filed 12 January 2005 with respect to the rejection of claims 16, 19, 22 have been fully considered but they are not persuasive.

Regarding claim 16, the applicant's arguments are moot in view of the new grounds of rejection.

Regarding the rejection of claims 19, 22 under 35 U.S.C. 103(a) as being unpatentable over Bronner et al. (US 5,792,703) in view of Psaras et al. (US 4,803,539), the applicant argues that the combination of Bronner et al. and Psaras et al. lack a layer of ruthenium, iridium, osmium, or platinum, since the rhodium claim limitation has been deleted from the group as currently set forth in both claims. However, as indicated in the above rejection, Psaras et al. also teach that Pt_2Si can be used as an alternative to Rh_2Si .

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS

Stephen W. Smoot
Patent Examiner
Art Unit 2813